# **CprE 381, Computer Organization and**

# **Assembly Level Programming**

# **Team Contract – Project Part 1**

Project Teams Group: \_\_\_\_\_\_\_\_\_\_\_\_\_3\_\_\_\_\_\_\_\_\_\_\_\_

Team Members: \_\_\_\_\_\_\_\_\_\_\_\_Zach Scurlock\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_Connor Hand\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Course Goals:**

* get an A in the course
* learn everything about computer architecture
* be able to explain the working of a stored-program computer from gates to C
* minimize the number of lost points

**Team Expectations:**

* **Conduct:** Communicate effectively and work efficiently on the project.
* **Communication:** Most communication will be in-person (roommates). Communication should occur daily and a response should be instant.
* **Group conventions:**Use capitals at start of words (i.e. AddSub) and add \_tb at the end when it is a testbench. Make testbenches for individual component when testing is necessary. Use google drive to sort code files and do version control.
* **Meetings:** We will use the VM from our apartment and work on the project often. Our team will meet every day because we live together.
* **Peer Evaluation Criteria:**Effort and contribution are mostly defined by the time spent on the project, but also on how important the contributions are.

**Role Responsibilities:**

| **Lab Part** | **Estimated Time** | **Design** | | **Test** | |
| --- | --- | --- | --- | --- | --- |
| **Lead** | **Timeline** | **Lead** | **Timeline** |
| High-level design | 1 hr | Zach | 9 | Connor | 10 |
| Test programs | 4 hr | Connor | 11 | Zach | 12 |
| Control logic | 2 hr | Zach | 7 | Connor | 8 |
| Fetch logic | 3 hr | Connor | 5 | Zach | 6 |
| Barrel shifter | 2 hr | Zach | 1 | Connor | 2 |
| ALU integration + Misc updates | 2 hr | Connor | 3 | Zach | 4 |
| High-level integration | 4 hr | Zach | 13 | Connor | 14 |
| Synthesis (human effort) | 1.5 hr | Connor | 15 | Zach | 16 |

**Integrity of Work:** *Do not delete the following.* We agree that the work we provide to other team members and ultimately submit for a grade is a direct result of our own work as described in the course syllabus. Specifically, we will generate all VHDL code ourselves and not copy VHDL code from online sources, other groups, book companion material, or past student projects to which anyone outside of my team has contributed.

**Student Signature** \_\_\_\_\_\_\_\_\_\_\_\_Zachary Scurlock\_\_\_ **Date** 9/27/2023

**Student Signature** \_\_\_\_\_\_\_\_\_\_\_\_Connor Hand\_\_\_\_\_\_\_\_ **Date** 9/27/2023